A METHOD, COMPUTER READABLE STORAGE MEDIUM AND COMPUTING DEVICE FOR CONVERTING A VECTOR VIDEO SIGNAL INTO A RASTER VIDEO SIGNAL

FIELD OF THE INVENTION

The present invention relates generally to the field of video format conversion which is applicable to industries such as simulation, avionic and industrial. More specifically the invention allows stroke video signals to be converted in real-time to a digital raster video using limited system resources allowing for modern digital video equipment to interface with legacy Cathode Ray Tube (CRT) systems.

BACKGROUND

Any discussion of the background art throughout the specification should in no way be considered as an admission that such background art is prior art nor that such background art is widely known or forms part of the common general knowledge in the field in Australia or worldwide.

Early computer display systems (such as those developed in the 1960s and 1970s) employed vector / stroke graphic displays where symbols were drawn by deflecting an electronic beam across a phosphor coated surface of the cathode ray tube (CRT). The position of the electronic beam was controlled by two analogue deflection voltages: X and Y.

Such vector display systems had advantages in requiring only a small amount of memory to generate images especially when considering the limited memory resources of early computing devices.

Vector display systems found a wide application in avionic display systems, such systems typically been characterised by limited computational and memory resources. Further, given the typically geometrical (vector) nature of avionics displays, vector display systems were capable of achieving high quality images, while utilising little memory and computing resources.

The design of aircraft models comprising of vector display technology, ceased only in 2000’s. These aircraft are expected to remain in service for at least a further 15 to 20 years.

However, CRT displays have an operational lifespan that is shorter than that of an aircraft. As time goes by, these CRT displays must be repaired and replaced. However, as
components become obsolete, it is becoming more difficult and expensive to maintain and replace CRT based avionics displays.

As such, a need therefore exists to replace CRT displays with modern digital displays. Where a display is been replaced in a safety critical applications such as avionics or medical systems, the approach described in this invention favours an ability to demonstrate regulatory compliance for measurement and testing requirements. Modern computer graphics systems are based on raster technology wherein an image is formed by discrete horizontal lines consisting of discrete pixels. In this manner, image data is stored into a video buffer memory and is retrieved line-by-line for display onto a raster display device. As such, raster technology suffers from the disadvantage of requiring memory and computational resources not supported by legacy avionics systems. Furthermore, it would be too expensive to replace the entire aircraft’s legacy system with one having memory and computational resources required to support modern raster displays.

Several attempts have been made to address this replacement of CRT technology with LCD. However, these attempts suffer from several disadvantages, including the introduction of visual artefacts (bright spots at line intersections, line pixilation and smoothing defects), requiring significant memory and computational resources to overcome. Furthermore, real-time conversion requirements only serve to increase the complexity of such converters thereby reducing the reliability of such converters.

Other existing arrangements attempting to convert video signals for display on raster display devices also suffer from disadvantages. For example, US Patent 6,496,160 describes a method to improve the quality of the resulting image of the stroke-to-raster converter by increasing the resolution, processing the image at a higher resolution and then down sampling the resolution in accordance with the size of the display device.


Systems such as these require large memory and computational resources due to the digital processing involved including in the scaling of the video signal. Also additional processing may lead to generating artefacts not present in source signal.

As such, a need therefore exists for a vector to raster video signal converter for converting the legacy analogue vector (stroke) video signals into digital raster signals for display in new
generation digital devices without consuming system memory and computational resources, yet providing a high resolution output.

The present invention seeks to provide a vector to raster video display converter, which will overcome or substantially ameliorate at least some of the deficiencies of the existing technology, or to at least provide an alternative.

It is to be understood that, if any existing technology is referred to herein, does not constitute an admission that the information forms part of the common general knowledge in that technology, in Australia or any other country.

SUMMARY

According to one aspect, there is provided a method, computer readable storage medium and computing device for converting a vector video signal into a raster video signal, the method comprising receiving X and Y vector deflection signals, generating a raster matrix in accordance with the X and Y vector deflection signals, the raster matrix being N x M, and generating a raster video signal in accordance with the raster matrix.

The analogue deflection signals may contain a mixture of stroke and raster information. The method may comprise converting the analogue deflection signals into raster display information using a robust and easily certifiable technique. The system is kept simple and low in functionality with no predictive algorithm used to analyse or determine input data type hence providing a system that is easier to test and demonstrate assurance in safety critical applications.

Preferably, the method further comprises scaling the raster matrix to a scaled raster matrix being \( N_1 \times M_1 \).

Preferably, \( N_1 > N \).

Preferably, \( M_1 > M \).

Preferably, scaling the raster matrix comprises interpolation.

Preferably, the interpolation comprises one of bilinear and bi-cubic interpolation.

Preferably, scaling the raster matrix comprises scaling the raster matrix in accordance with resolution configuration settings representing at least one of \( N_1 \) and \( M_1 \).

Preferably, the method is a field-programmable gate array (FPGA) or programmable logic array (PLA) implemented method.
Preferably, the method further comprises sampling the X and Y vector deflection signals to produce sampled X and Y vector deflection signals.

Preferably, the method further comprises filtering the sampled X and Y vector deflection signals.

Preferably, the filtering comprises low pass filtering.

Preferably, generating the raster matrix comprises pixel mapping.

Preferably, the pixel mapping comprises mapping the X and Y vector deflection signals to the raster matrix.

Preferably, pixel mapping comprises mapping the X vector deflection signal to a column of the raster matrix and mapping the Y vector deflection signal to a row of the raster matrix.

Preferably, the raster matrix comprises binary data elements.

Preferably, pixel mapping comprises setting a data elements corresponding to the column and the row to 1.

Preferably, the method further comprises generating a further raster matrix in accordance with the X and Y vector deflection signals, the further raster matrix being NxF; and generating the raster video signal in accordance with the raster matrix and the further raster matrix.

Preferably, the method further comprises generating a weighted raster matrix in accordance with the raster matrix and the further raster matrix; and generating the raster video signal in accordance with the weighted raster matrix.

Preferably, generating a weighted raster matrix comprises summing the raster matrix and the further raster matrix.

Preferably, the method further comprises generating an averaged raster matrix in accordance with the weighted raster matrix; and generating the raster video signal in accordance with the averaged raster matrix.

Preferably, the method further comprises generating a further n raster matrices in accordance with the X and Y vector deflection signals, the further raster matrices being NxF; and generating the raster video signal in accordance with the further n raster matrices.

Preferably, the method further comprises selecting a value for n in accordance with a desired throughput rate.
Preferably, the method further comprises storing the raster matrix in a frame buffer.

According to another aspect, there is provided a computing device for converting a vector video signal into a raster video signal. The computing device comprising a processor for processing digital data; an analogue to digital converter for sampling X and Y deflection signals, the analogue to digital converter being operably coupled to the processor; and a video interface for outputting a raster video signal to a raster display device, the video interface being operably coupled to the processor, wherein in use, the processor is controlled to receive, via the analogue to digital converter, the X and Y vector deflection signals, generate a raster matrix in accordance with the X and Y vector deflection signals, the raster matrix being NxM, generate the raster video signal in accordance with the raster matrix; and output, via the video interface, the raster video signal.

Preferably, the processor is further controlled to scale the raster matrix to a scaled raster matrix being N1xM1.

Preferably, N1 > N.

Preferably, M1 > M.

Preferably, scaling the raster matrix comprises interpolation.

Preferably, the interpolation comprises one of bilinear and bi-cubic interpolation.

Preferably, scaling the raster matrix comprises scaling the raster matrix in accordance with resolution configuration settings representing at least one of N1 and M1.

Preferably, the computing device is a FPGA or PLA device.

Preferably, the processor is further controlled to sampling the X and Y vector deflection signals to produce sampled X and Y vector deflection signals.

Preferably, the processor is further controlled to filter the sampled X and Y vector deflection signals.

Preferably, filtering comprises a low pass filtering.

Preferably, generating the raster matrix comprises pixel mapping.

Preferably, the pixel mapping comprises mapping the X and Y vector deflection signals to the raster matrix.
Preferably, pixel mapping comprises mapping the X vector deflection signal to a column of the raster matrix and mapping the Y vector deflection signal to a row of the raster matrix.

Preferably, the raster matrix comprises binary data elements.

Preferably, pixel mapping comprises setting a data element corresponding to the column and the row to 1.

Preferably, the processor is further controlled to generate a further raster matrix in accordance with the X and Y vector deflection signals, the further raster matrix being NxM; and generate the raster video signal in accordance with the raster matrix and the further raster matrix.

Preferably, the processor is further controlled to generate a weighted raster matrix in accordance with the raster matrix and the further raster matrix; and generate the raster video signal in accordance with the weighted raster matrix.

Preferably, generate a weighted raster matrix comprises summing the raster matrix and the further raster matrix.

Preferably, the processor is further controlled to generate an averaged raster matrix in accordance with the weighted raster matrix; and generate the raster video signal in accordance with the averaged raster matrix.

Preferably, the processor is further controlled to generate a further n raster matrices in accordance with the X and Y vector deflection signals, the further raster matrices being NxM; and generate the raster video signal in accordance with the further n raster matrices.

Preferably, the processor is further controlled to selecting a value for n in accordance with a desired throughput rate.

Preferably, the processor is further controlled to storing the raster matrix in a frame buffer.

According to a second aspect, there is provided a computer readable storage medium comprising computer code instructions executable by a computing device for converting a vector video signal into a raster video signal. The computer readable storage medium comprising instructions for receiving, via the analogue to digital converter, the X and Y vector deflection signals, generating a raster matrix in accordance with the X and Y vector deflection signals, the raster matrix being NxM, generating the raster video signal in accordance with the raster matrix; and outputting, via the video interface, the raster video signal.
Preferably, the computer readable storage medium further comprises instructions for scaling the raster matrix to a scaled raster matrix being N1xM1.

Preferably, N1 > N.

Preferably, M1 > M.

Preferably, scaling the raster matrix comprises interpolation.

Preferably, the interpolation comprises one of bilinear and bi-cubic interpolation.

Preferably, scaling the raster matrix comprises scaling the raster matrix in accordance with resolution configuration settings representing at least one of N1 and M1.

Preferably, the computer readable storage medium is executable by a FPGA or PLA device.

Preferably, the computer readable storage medium further comprises instructions for sampling the X and Y vector deflection signals to produce sampled X and Y vector deflection signals.

Preferably, the computer readable storage medium further comprises instructions for filtering the sampled X and Y vector deflection signals.

Preferably, filtering comprises a low pass filtering.

Preferably, generating the raster matrix comprises pixel mapping.

Preferably, the pixel mapping comprises mapping the X and Y vector deflection signals to the raster matrix.

Preferably, pixel mapping comprises mapping the X vector deflection signal to a column of the raster matrix and mapping the X vector deflection signal to a row of the raster matrix.

Preferably, the raster matrix comprises binary data elements.

Preferably, pixel mapping comprises setting a data elements corresponding to the column and the row to 1.

Preferably, the computer readable storage medium further comprises instructions for generating a further raster matrix in accordance with the X and Y vector deflection signals, the further raster matrix being NxM; and generating the raster video signal in accordance with the raster matrix and the further raster matrix.
Preferably, the computer readable storage medium further comprises instructions for generating a weighted raster matrix in accordance with the raster matrix and the further raster matrix; and generating the raster video signal in accordance with the weighted raster matrix.

Preferably, generating a weighted raster matrix comprises summing the raster matrix and the further raster matrix.

Preferably, the computer readable storage medium further comprises instructions for generating an averaged raster matrix in accordance with the weighted raster matrix; and generating the raster video signal in accordance with the averaged raster matrix.

Preferably, the computer readable storage medium further comprises instructions for generating a further n raster matrices in accordance with the X and Y vector deflection signals, the further raster matrices being NxM; and generating the raster video signal in accordance with the further n raster matrices.

Preferably, the computer readable storage medium further comprises instructions for selecting a value for n in accordance with a desired throughput rate.

Preferably, the computer readable storage medium further comprises instructions for storing the raster matrix in a frame buffer.

According to a third aspect, there is provided an apparatus and method for converting analogue deflection signals containing mixture of raster and stroke display information into raster scan image display. The apparatus may comprise sampling circuitry having resolution sufficient enough to produce pixel data representing pixel or sub-pixel locations and a sampling rate that is high enough to digitize high speed raster part of the frame. The apparatus may further comprise a pixel mapping module that counts the number of occurrences of analogue illumination at particular locations of the image. The apparatus may further comprise a frame buffer containing brightness information for every sub-pixel location and every fundamental colour (e.g. red, green, and blue). The apparatus may further comprise an averaging module that calculates sliding average of several frames to emulate phosphor persistence of the analogue deflection signals. The apparatus may further comprise a video scaling module to produce raster image of desired resolution. The apparatus may further comprise a filter to further reduce noise in the output image.

According to an arrangement of the third aspect, there is provided an apparatus and method for converting analogue deflection signals containing mixture of raster and stroke display information into raster scan image display, comprising: sampling circuitry having resolution
sufficient enough to produce pixel data representing pixel or sub-pixel locations and sampling rate high enough to digitize high speed raster part of the frame; a pixel mapping module that counts the number of occurrences of analogue illumination at particular locations of the image; a frame buffer containing brightness information for every sub-pixel location and every fundamental colour (e.g. red, green, and blue); an averaging module that calculates sliding average of several frames to emulate phosphor persistence of the analogue deflection signals; a video scaling module to produce raster image of desired resolution; and a filter to further reduce noise in output image.

The sampling circuitry may be adapted to sample X and Y deflection signals. The sampling rate may be selected to be high enough to digitize fast changing raster part of the frame.

The pixel mapping module may be adapted for converting digitized samples into pixel or sub-pixel locations based on number of occurrences per frame.

The frame buffer may be adapted for storing temporary pixel or sub-pixel data and for supporting the process of averaging of several frames for emulating a phosphor persistence.

The averaging module may be adapted for emulating a phosphor persistence.

The video scaling module may be adapted to produce image of desired resolution in accordance to resolution of target raster scan display.

The filter may be adapted to further reduce noise in the output image.

Other aspects of the invention are also disclosed.

**BRIEF DESCRIPTION OF THE DRAWINGS**

Notwithstanding any other forms which may fall within the scope of the present invention, a preferred embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

**Figure 1** shows an apparatus 100 for converting a vector video signal to a raster video signal in accordance with an embodiment of the present invention – apparatus 100 may be either a computing device or a programmable hardware device such as, for example, a field-programmable gate array (FPGA) or programmable logic array (PLA) device;

**Figure 2** shows a functional schematic 200 for converting vector video signals to raster video signals in accordance with an embodiment of the present invention;
**Figure 3.** shows a functional schematic of the functions performed by the computing device 100 in converting a vector video signal to a raster video signal in accordance with an embodiment of the present invention; and

**Figure 4** shows the apparatus of **Figure 1** having created several raster matrices, summing the several raster matrices using sum module to form weighted raster matrix, representing how frequently the electron beam would hit the phosphor at every particular position in accordance with an embodiment of the present invention.

**DESCRIPTION OF EMBODIMENTS**

It should be noted in the following description, that like or the same referenced numerals in different embodiments denote the same or similar features.

There is disclosed herein a method and apparatus / computing device (such as an a field-programmable gate array (FPGA) or programmable logic array (PLA) device or equivalent) for converting a vector video signal to a raster video signal. The analogue deflection signals of the vector video signal may contain a mixture of stroke and raster information. The method may comprise converting the analogue deflection signals into raster display information using a robust and easily certifiable technique. The system is kept simple and low in functionality with no predictive algorithm used to analyse or determine input data type hence a system easier to test and demonstrate assurance in safety critical applications.

Analogue deflection signals containing stroke and raster information in single frame are treated as purely stroke information and no analysis is being performed in order to identify, recognize or process raster information separately from stroke information.

The apparatus includes sampling circuitry to convert analogue signals into pixel or sub-pixel locations. Brightness information is calculated based on the amount of coverage and time the electronic beam spends in particular location.

One application of the embodiments described herein is for retrofitting modern digital display devices to legacy vector - based aeronautic systems. However, the embodiments may have a wider application also.

As will be described in further detail below, the embodiments described herein do not drain the memory (i.e. RAM resources) and computational resources of the existing legacy system. But rather employs introduced memory and competition resources. For example, where the embodiments are implemented using an FPGA or PLA, the generation of the raster matrix
and the like (as will be described in further detail below) will be calculated using the FPGA, PLA or processor and stored using a memory device associated with the FPGA, PLA, or processor. In this manner, high-resolution raster video signals may be produced by the embodiments described herein without draining system resources.

Furthermore, in employing introduced memory (such as the FPGA or PLA’s memory) there is avoided the possibility of corruption as compared to utilisation of an external memory device. Furthermore, utilisation of the FPGA or PLAs internal memory decreases access times allowing for a faster implementation.

However, it should be noted that in certain embodiments, the computing device may be adapted for utilising external memory resources. Yet further, the method described herein may be implemented by an existing computing system.

*Computing device*

*Figure 1* shows an apparatus 100 for converting a vector video signal to a raster video signal. Apparatus 100 may be a computing device. In a preferred embodiment, the computing device 100 is an FPGA or PLA device. However, it should be noted that the functionality described herein may be implemented by a computing device/s 100 of other types.

The computing device 100 comprises of memory 110 which may comprise volatile memory (RAM) and / or non-volatile memory (ROM). Typically the memory 110 comprises a combination of volatile and non-volatile memory, such that the non-volatile memory stores the computing device 100 firmware and the volatile memory stores one or more temporary results of the fetch-decode-execute cycle, as described below.

Typically, a computer program code is preloaded into the memory 100. However, the computer program code instructions may be loaded into the memory 110 from the storage medium using a storage medium reader or from a network.

The computing device 100 comprises of an arithmetic logic unit or processor 105 for the execution of computer program code instructions. The processor 105 is typically a low-power microprocessor suited for low power computing device applications. During the bootstrap phase, an operating system and one or more software applications are loaded the memory 110. During the fetch-decode-execute cycle, the processor 105 fetches computer program code instructions from memory 110, decodes the instructions into machine code, executes the instructions and stores the results in the memory 110.
The computing device 100 also comprises of a video interface 115 for outputting raster-based video signals for display on a raster-based display device 120. The display device 120 may take the form of any raster-based display device including a liquid crystal display (LCD) or similar display device.

The computing device 100 further comprises an analogue to digital (A/D) converter 1030 for sampling X and Y deflection signals 135 received from a vector-based system.

The computing device 100 also comprises a communication bus 150 for interconnecting the various devices described above.

As will be described in further detail below, the computing device 100 is controlled by the computer program code to sample the X and Y deflection signals 135 for the purposes of creating a plurality of raster matrices for storage in a video buffer in memory 110. The computing device 100 generates the raster-based video signals for display on the raster-based display 120 by reading values calculated from the plurality of raster matrices stored in memory 110.

Functional schematic

Referring now to Figure 2, there is shown a functional schematic 200 for converting vector video signals to raster video signals.

Specifically, the schematic 200 shows the receipt of vector deflection signals 205 X and Y, such as those received from a legacy avionics system. The schematic 100 comprises a vector to raster converter 210 adapted for converting the X and Y deflection signals 205 into a plurality of raster matrices having dimensions NxM.

The schematic 200 further comprises a video scaler 215 for scaling the NxM resolution raster values to N1xM1 resolution. The confidential processing of the raster matrices (as will be described in further detail below) is advantageously at the lower NxM resolution which are subsequently interpolated to greater resolution N1xM1. In this manner, computational and memory resources are preserved in utilising the lower resolution image.

The video scaler 205 allows for the provision of differing resolutions without impact on performance. Image quality is preserved by utilising an interpolation technique to a sample the NxM resolution raster matrices to the N1xM1 resolution raster matrices. Such interpolation may comprise of bilinear, bi-cubic, or any other interpolation technique.
The schematic 200 further comprises of a raster-based display device 220 such as an LCD display, for the display of the output raster video signals.

**Computing device for converting a vector video signal to a raster video signal**

Turning now to **Figure 3**, there is shown a functional schematic of the functions performed by the computing device 100 in converting a vector video signal to a raster video signal.

Deflection signals X and Y 305 are each sampled by A/D converter 130 which sampled signals are subsequently filtered by digital filters 310 to eliminate noise outside the signal frequency range, by using digital bandpass, lowpass filtering and the like.

The filtered signals are supplied to the input of the pixel mapping module 315. The pixel mapping module 315 generates a plurality of raster matrices in accordance with the X and Y deflection signals for storage in the video buffer 320 which comprises a plurality of raster matrices (otherwise known as raster frames).

The pixel mapping module 315 populates a binary representation raster matrix 405 in accordance with the deflection signals X and Y for storage in frame buffer 320. Specifically, the pixel mapping module 315 calculates a column and a row of a raster matrix 405 for population in accordance with the X and Y deflection signals. For each matrix element corresponding to the calculated column and row of the raster matrix 405, the pixel mapping module 315 updates the element of value to 1, wherein the remaining elements are assigned values of zero. In this manner, the raster matrix 405 comprises a binary representation substantially corresponding to the position of the electron beam on the phosphor of the CRT display.

Once a raster matrix 405 is filled, another is populated, and so on and so forth. In this manner, a plurality of raster matrices 405 are created in accordance with the X and Y deflection signals.

Turning now to **Figure 4**, there is shown, the computing device 100 having created several raster matrices 405, summing the several raster matrices using sum module 325 to form weighted raster matrix 410, representing how frequently the electron beam would hit the phosphor at every particular position. Specifically, in **Figure 4**, there is shown a plurality of raster matrices 405, wherein these plurality of raster matrices are summed to calculate weighted raster matrix 410.
It should be noted that while 3 raster matrices 405 (and associated frame buffers 320) are given in the accompanying figures, it should be noted that any number of raster matrices 405 may be utilised. In this regard, having several frame buffers increases the throughput of the system advantageous for real time performance.

Then, having calculated the weighted raster matrix 410, the computing device 100 averages the weighted raster matrix 410 to form averaged raster matrix 415 to reduce noise. In this manner, pixels with a low number of hits will be considered noise and will be eliminated.

It should be noted that the weighting and averaging is described with reference to Figure 4 may be performed upon receipt of every next raster matrix 405 wherein ‘n’ may be from 1 to m. Upon receipt of every next raster matrix 405, the oldest matrix is being discarded and new matrix is being stored in array. Therefore, moving average is being performed.

At the output of the weighting / sum module 325 and averaging module 330, the computing device 100 has a frame buffer having resolution N x M.

Now, in a preferred embodiment, the calculations performed thus far by the computing device 100 are performed at a lower resolution N x M so as to save on computational and memory requirements wherein the lower resolution N x M is subsequently scaled up to a display resolution N₁ x M₁ for display.

As such, schematic 300 comprises a video scaler 340 to scale the lower resolution N x M resolution raster matrix from the frame buffer 335 up to a high resolution raster matrix having dimensions N₁ x M₁ for storage in the output frame buffer 350 and outputs to the raster display 120.

The video scaler 340 may utilise an interpolation technique to generate the higher resolution output frame buffer 350. The interpolation technique utilised may comprise of bilinear, bi-cubic interpolation and the like.

So as to counter high frequencies introduced by the video scaler 340, the schematic 300 comprises 2D filter 345 to remove the high frequencies.

Advantages

As such, the embodiments described herein provide several advantages, including legacy image generation systems which utilize CRT display not having to be replaced in order to use a new display technology device such as LCD, LCOS, OLED etc. Furthermore, phosphor like video processing and representation reduces system complexity and maintains the
integrity of the video signal which is very important in reliability to critical systems, such as avionics systems. Yet further, there is a reduced usage of RAM resources in the stroke-to-raster conversion system wherein lower resolution leads to smaller amount of memory required for processing. Further, there is provided increased throughput capability wherein processing less amount of memory leads to improvement of real-time performance. Yet further there is provided video scalability for different display resolutions due to the ability to control the resolution.

**INTERPRETATION**

*Wireless:*

The invention may be embodied using devices conforming to other network standards and for other applications, including, for example other WLAN standards and other wireless standards. Applications that can be accommodated include IEEE 802.11 wireless LANs and links, and wireless Ethernet.

In the context of this document, the term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. In the context of this document, the term “wired” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a solid medium. The term does not imply that the associated devices are coupled by electrically conductive wires.

*Processes:*

Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as “processing”, “computing”, “calculating”, “determining”, “analysing” or the like, refer to the action and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities into other data similarly represented as physical quantities.
Processor:

In a similar manner, the term “processor” may refer to any device or portion of a device that processes electronic data, e.g., from registers and/or memory to transform that electronic data into other electronic data that, e.g., may be stored in registers and/or memory. A “computer” or a “computing device” or a “computing machine” or a “computing platform” may include one or more processors.

The methodologies described herein are, in one embodiment, performable by one or more processors that accept computer-readable (also called machine-readable) code containing a set of instructions that when executed by one or more of the processors carry out at least one of the methods described herein. Any processor capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken are included. Thus, one example is a typical processing system that includes one or more processors. The processing system further may include a memory subsystem including main RAM and/or a static RAM, and/or ROM.

Computer-Readable Medium:

Furthermore, a computer-readable carrier medium may form, or be included in a computer program product. A computer program product can be stored on a computer usable carrier medium, the computer program product comprising a computer readable program means for causing a processor to perform a method as described herein.

Networked or Multiple Processors:

In alternative embodiments, the one or more processors operate as a standalone device or may be connected, e.g., networked to other processor(s), in a networked deployment, the one or more processors may operate in the capacity of a server or a client machine in server-client network environment, or as a peer machine in a peer-to-peer or distributed network environment. The one or more processors may form a web appliance, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine.

Note that while some diagram(s) only show(s) a single processor and a single memory that carries the computer-readable code, those in the art will understand that many of the components described above are included, but not explicitly shown or described in order not to obscure the inventive aspect. For example, while only a single machine is illustrated, the term “machine” shall also be taken to include any collection of machines that individually or
jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies discussed herein.

Additional Embodiments:

Thus, one embodiment of each of the methods described herein is in the form of a computer-readable carrier medium carrying a set of instructions, e.g., a computer program that are for execution on one or more processors. Thus, as will be appreciated by those skilled in the art, embodiments of the present invention may be embodied as a method, an apparatus such as a special purpose apparatus, an apparatus such as a data processing system, or a computer-readable carrier medium. The computer-readable carrier medium carries computer readable code including a set of instructions that when executed on one or more processors cause a processor or processors to implement a method. Accordingly, aspects of the present invention may take the form of a method, an entirely hardware embodiment, an entirely software embodiment or an embodiment combining software and hardware aspects. Furthermore, the present invention may take the form of carrier medium (e.g., a computer program product on a computer-readable storage medium) carrying computer-readable program code embodied in the medium.

Carrier Medium:

The software may further be transmitted or received over a network via a network interface device. While the carrier medium is shown in an example embodiment to be a single medium, the term “carrier medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “carrier medium” shall also be taken to include any medium that is capable of storing, encoding or carrying a set of instructions for execution by one or more of the processors and that cause the one or more processors to perform any one or more of the methodologies of the present invention. A carrier medium may take many forms, including but not limited to, non-volatile media, volatile media, and transmission media.

Implementation:

It will be understood that the steps of methods discussed are performed in one embodiment by an appropriate processor (or processors) of a processing (i.e., computer) system executing instructions (computer-readable code) stored in storage. It will also be understood that the invention is not limited to any particular implementation or programming technique and that
the invention may be implemented using any appropriate techniques for implementing the functionality described herein. The invention is not limited to any particular programming language or operating system.

**Means for Carrying out a Method or Function**

Furthermore, some of the embodiments are described herein as a method or combination of elements of a method that can be implemented by a processor of a processor device, computer system, or by other means of carrying out the function. Thus, a processor with the necessary instructions for carrying out such a method or element of a method forms a means for carrying out the method or element of a method. Furthermore, an element described herein of an apparatus embodiment is an example of a means for carrying out the function performed by the element for the purpose of carrying out the invention.

**Connected**

Similarly, it is to be noticed that the term connected, when used in the claims, should not be interpreted as being limitative to direct connections only. Thus, the scope of the expression a device A connected to a device B should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B. It means that there exists a path between an output of A and an input of B which may be a path including other devices or means. “Connected” may mean that two or more elements are either in direct physical or electrical contact, or that two or more elements are not in direct contact with each other but yet still co-operate or interact with each other.

**Embodiments:**

Reference throughout this specification to “one embodiment” or “an embodiment”, or “an arrangement” means that a particular feature, structure or characteristic described in connection with the embodiment or arrangement is included in at least one embodiment or arrangement of the present invention. Thus, appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment, but may. Furthermore, the particular features, structures or characteristics may be combined in any suitable manner, as would be apparent to one of ordinary skill in the art from this disclosure, in one or more embodiments or arrangements.

Similarly it should be appreciated that in the above description of example embodiments or arrangements of the invention, various features of the invention are sometimes grouped together in a single embodiment, arrangement, figure, or description thereof for the purpose
of streamlining the disclosure and aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims following the Detailed Description of Specific Embodiments are hereby expressly incorporated into this Detailed Description of Specific Embodiments, with each claim standing on its own as a separate embodiment of this invention.

Furthermore, while some embodiments described herein include some but not other features included in other embodiments, combinations of features of different embodiments are meant to be within the scope of the invention, and form different embodiments, as would be understood by those in the art. For example, in the following claims, any of the claimed embodiments can be used in any combination.

Different Instances of Objects

As used herein, unless otherwise specified the use of the ordinal adjectives “first”, “second”, “third”, etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

Specific Details

In the description provided herein, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known methods, structures and techniques have not been shown in detail in order not to obscure an understanding of this description.

Terminology

In describing the preferred embodiment of the invention illustrated in the drawings, specific terminology will be resorted to for the sake of clarity. However, the invention is not intended to be limited to the specific terms so selected, and it is to be understood that each specific term includes all technical equivalents which operate in a similar manner to accomplish a similar technical purpose. Terms such as “forward”, “rearward”, “radially”, “peripherally”, “upwardly”, “downwardly”, and the like are used as words of convenience to provide reference points and are not to be construed as limiting terms.
Comprising and Including

In the claims which follow and in the preceding description of the invention, except where the context requires otherwise due to express language or necessary implication, the word “comprise” or variations such as “comprises” or “comprising” are used in an inclusive sense, i.e. to specify the presence of the stated features but not to preclude the presence or addition of further features in various embodiments of the invention.

Any one of the terms: including or which includes or that includes as used herein is also an open term that also means including at least the elements/features that follow the term, but not excluding others. Thus, including is synonymous with and means comprising.

Scope of Invention

Thus, while there has been described what are believed to be the preferred embodiments of the invention, those skilled in the art will recognize that other and further modifications may be made thereto without departing from the spirit of the invention, and it is intended to claim all such changes and modifications as fall within the scope of the invention. For example, any formulas given above are merely representative of procedures that may be used.

Functionality may be added or deleted from the block diagrams and operations may be interchanged among functional blocks. Steps may be added or deleted to methods described within the scope of the present invention.

Although the invention has been described with reference to specific examples, it will be appreciated by those skilled in the art that the invention may be embodied in many other forms.

Industrial Applicability

It is apparent from the above, that the arrangements described are applicable to the electronics display industries.
Claims

1. A method of converting a vector video signal into a raster video signal, the vector video signal comprising analogue deflection signals comprising a mixture of raster and stroke display information, the method comprising:

receiving X and Y vector deflection signals;

generating a raster matrix in accordance with the X and Y vector deflection signals, the raster matrix being NxM;

generating a further raster matrix in accordance with the X and Y vector deflection signals, the further raster matrix being NxM;

generating a weighted raster matrix in accordance with the raster matrix and the further raster matrix; and

generating a raster video signal in accordance with the weighted raster matrix;

wherein the raster video signal comprises binary data elements.

2. A method as claimed in claim 1, further comprising scaling the raster matrix to a scaled raster matrix being N1xM1.

3. A method as claimed in claim 2, wherein N1 > N.

4. A method as claimed in claim 2, wherein M1 > M.

5. A method as claimed in claim 2, wherein scaling the raster matrix comprises interpolation.

6. A method as claimed in claim 5, wherein the interpolation comprises one of bilinear and bi-cubic interpolation.

7. A method as claimed in claim 2, wherein scaling the raster matrix comprises scaling the raster matrix in accordance with resolution configuration settings representing at least one of N1 and M1.

8. A method as claimed in claim 1, wherein the method is a FPGA or PLA implemented method.

9. A method as claimed in claim 1, further comprising sampling the X and Y vector deflection signals to produce sampled X and Y vector deflection signals.
10. A method as claimed in claim 10, further comprising filtering the sampled X and Y vector deflection signals.

11. A method as claimed in claim 10, wherein the filtering comprises low pass filtering.

12. A method as claimed in claim 1, wherein generating the raster matrix comprises pixel mapping.

13. A method as claimed in claim 12, wherein the pixel mapping comprises mapping the X and Y vector deflection signals to the raster matrix.

14. A method as claimed in claim 13, wherein pixel mapping comprises mapping the X vector deflection signal to a column of the raster matrix and mapping the Y vector deflection signal to a row of the raster matrix.

15. A method as claimed in claim 1, wherein pixel mapping comprises setting a data elements corresponding to the column and the row to 1.

16. A method as claimed in claim 1, wherein generating a weighted raster matrix comprises summing the raster matrix and the further raster matrix.

17. A method as claimed in claim 1, further comprising:

   generating an averaged raster matrix in accordance with the weighted raster matrix;

   and

   generating the raster video signal in accordance with the averaged raster matrix.

18. A method as claimed in claim 1, further comprising:

   generating a further n raster matrices in accordance with the X and Y vector deflection signals, the further raster matrices being NxM; and

   generating the raster video signal in accordance with the further n raster matrices.

19. A method as claimed in claim 18, further comprising selecting a value for n in accordance with a desired throughput rate.

20. A method as claimed in claim 1, further comprising storing the raster matrix in a frame buffer.

21. An apparatus for converting a vector video signal into a raster video signal, the vector video signal comprising analogue deflection signals comprising a mixture of raster and stroke display information, the computing device comprising:
a processor for processing digital data;

an analogue to digital converter for sampling the analogue X and Y deflection signals, the analogue to digital converter being operably coupled to the processor and to a pixel mapping module adapted to produce pixel data representing pixel or sub-pixel locations

a frame buffer comprising brightness information for each sub-pixel location and each fundamental display colour

an averaging module adapted for calculating a sliding average of several frames of the raster video signal to emulate phosphor persistence

a video scaling module adapted to produce a raster image of resolution N x M; and

a video interface for outputting a raster video signal to a raster display device, the video interface being operably coupled to the processor, wherein in use, the processor is controlled to:

receive, via the analogue to digital converter, the X and Y vector deflection signals,

generate a raster matrix in accordance with the X and Y vector deflection signals, the raster matrix being N x M,

generate the raster video signal in accordance with the raster matrix; and

output, via the video interface, the raster video signal.

22. An apparatus as claimed in claim 21, wherein the processor is further controlled to scale the raster matrix to a scaled raster matrix being N1 x M1.

23. An apparatus as claimed in claim 22, wherein N1 > N.

24. An apparatus as claimed in claim 22, wherein M1 > M.

25. An apparatus as claimed in claim 22, wherein scaling the raster matrix comprises interpolation.

26. An apparatus as claimed in claim 25, wherein the interpolation comprises one of bilinear and bi-cubic interpolation.

27. An apparatus as claimed in claim 22, wherein scaling the raster matrix comprises scaling the raster matrix in accordance with resolution configuration settings representing at least one of N1 and M1.
28. An apparatus as claimed in claim 21, wherein the computing device is a FPGA or PLA device.

29. An apparatus as claimed in claim 21, wherein the processor is further controlled to sampling the X and Y vector deflection signals to produce sampled X and Y vector deflection signals.

30. An apparatus as claimed in claim 29, wherein the processor is further controlled to filter the sampled X and Y vector deflection signals.

31. An apparatus as claimed in claim 30, wherein filtering comprises a low pass filtering.

32. An apparatus as claimed in claim 21, wherein generating the raster matrix comprises pixel mapping.

33. An apparatus as claimed in claim 32, wherein the pixel mapping comprises mapping the X and Y vector deflection signals to the raster matrix.

34. An apparatus as claimed in claim 33, wherein pixel mapping comprises mapping the X vector deflection signal to a column of the raster matrix and mapping the X, Y vector deflection signal to a row of the raster matrix.

35. An apparatus as claimed in claim 32, wherein the raster matrix comprises binary data elements.

36. An apparatus as claimed in claim 35, wherein pixel mapping comprises setting a data elements corresponding to the column and the row to 1.

37. An apparatus as claimed in claim 21, wherein the processor is further controlled to:

   generate a further raster matrix in accordance with the X and Y vector deflection signals, the further raster matrix being NxM; and

   generate the raster video signal in accordance with the raster matrix and the further raster matrix.

38. An apparatus as claimed in claim 37, wherein the processor is further controlled to:

   generate a weighted raster matrix in accordance with the raster matrix and the further raster matrix; and

   generate the raster video signal in accordance with the weighted raster matrix.
39. An apparatus as claimed in claim 38, wherein generate a weighted raster matrix comprises summing the raster matrix and the further raster matrix.

40. An apparatus as claimed in claim 38, wherein the processor is further controlled to:

   generate an averaged raster matrix in accordance with the weighted raster matrix; and

   generate the raster video signal in accordance with the averaged raster matrix.

41. 44. An apparatus as claimed in claim 21, wherein the processor is further controlled to:

   generate a further n raster matrices in accordance with the X and Y vector deflection signals, the further raster matrices being NxM; and

   generate the raster video signal in accordance with the further n raster matrices.

42. 45. An apparatus as claimed in claim 44, wherein the processor is further controlled to selecting a value for n in accordance with a desired throughput rate.

43. An apparatus as claimed in claim 21, wherein the processor is further controlled to storing the raster matrix in a frame buffer.

44. An apparatus as claimed in claim 21, further comprising a filter to further reduce noise in the output raster video signal.

45. An apparatus as claimed in claim 21, wherein the analogue to digital converter for sampling the analogue X and Y deflection signals comprises a sampling rate adapted for digitizing fast changing raster parts in each frame of the video signal.

46. An apparatus as claimed in claim 21, wherein the pixel mapping module is adapted for converting digitized samples into pixel or sub-pixel locations based on the number of occurrences per frame.

47. An apparatus as claimed in claim 21, wherein the frame buffer is adapted for storing temporary pixel or sub-pixel data and for supporting the process of averaging of several frames for emulating a phosphor persistence.

48. An apparatus as claimed in claim 21, wherein the video scaling module is adapted to produce image of resolution NxM in accordance with the resolution of a target raster scan display screen.
49. A computer readable storage medium comprising computer code instructions executable by a computing device for converting a vector video signal into a raster video signal, the vector video signal comprising analogue deflection signals comprising a mixture of raster and stroke display information, the computer readable storage medium comprising instructions for:

- receiving, via the analogue to digital converter, the analogue X and Y vector deflection signals,
- generating a raster matrix in accordance with the analogue X and Y vector deflection signals, the raster matrix being NxM,
- generating a further raster matrix in accordance with the X and Y vector deflection signals, the further raster matrix being NxM;
- generating a weighted raster matrix in accordance with the raster matrix and the further raster matrix;
- generating the raster video signal in accordance with the weighted raster matrix, wherein the raster matrix comprises binary data elements; and
- outputting, via the video interface, the raster video signal.

50. A computer readable storage medium as claimed in claim 49, further comprising instructions for scaling the raster matrix to a scaled raster matrix being N1xM1.

51. A computer readable storage medium as claimed in claim 50, wherein N1 > N.

52. A computer readable storage medium as claimed in claim 50, wherein M1 > M.

53. A computer readable storage medium as claimed in claim 50, wherein scaling the raster matrix comprises interpolation.

54. A computer readable storage medium as claimed in claim 53, wherein the interpolation comprises one of bilinear and bi-cubic interpolation.

55. A computer readable storage medium as claimed in claim 50, wherein scaling the raster matrix comprises scaling the raster matrix in accordance with resolution configuration settings representing at least one of N1 and M1.

56. A computer readable storage medium as claimed in claim 49, wherein the computer readable storage medium is executable by a FPGA or PLA device.
57. A computer readable storage medium as claimed in claim 49, further comprising
instructions for sampling the X and Y vector deflection signals to produce sampled X and Y
vector deflection signals.

58. A computer readable storage medium as claimed in claim 57, further comprising
instructions for filtering the sampled X and Y vector deflection signals.

59. A computer readable storage medium as claimed in claim 58, wherein filtering
comprises a low pass filtering.

60. A computer readable storage medium as claimed in claim 49, wherein generating the
raster matrix comprises pixel mapping.

61. A computer readable storage medium as claimed in claim 60, wherein the pixel
mapping comprises mapping the X and Y vector deflection signals to the raster matrix.

62. A computer readable storage medium as claimed in claim 60, wherein pixel mapping
comprises mapping the X vector deflection signal to a column of the raster matrix and
mapping the X Y vector deflection signal to a row of the raster matrix.

63. A computer readable storage medium as claimed in claim 60, wherein the raster
matrix comprises binary data elements.

64. A computer readable storage medium as claimed in claim 63, wherein pixel mapping
comprises setting a data elements corresponding to the column and the row to 1.

65. A computer readable storage medium as claimed in claim 49, further comprising
instructions for:

- generating a further raster matrix in accordance with the X and Y vector deflection
  signals, the further raster matrix being N x M; and
- generating the raster video signal in accordance with the raster matrix and the further
  raster matrix.

66. A computer readable storage medium as claimed in claim 65, further comprising
instructions for:

- generating a weighted raster matrix in accordance with the raster matrix and the
  further raster matrix; and
- generating the raster video signal in accordance with the weighted raster matrix.
67. A computer readable storage medium as claimed in claim 66, wherein generating a weighted raster matrix comprises summing the raster matrix and the further raster matrix.

68. A computer readable storage medium as claimed in claim 66, further comprising instructions for:

- generating an averaged raster matrix in accordance with the weighted raster matrix; and
- generating the raster video signal in accordance with the averaged raster matrix.

69. A computer readable storage medium as claimed in claim 49, further comprising instructions for:

- generating a further n raster matrices in accordance with the X and Y vector deflection signals, the further raster matrices being NxM; and
- generating the raster video signal in accordance with the further n raster matrices.

70. A computer readable storage medium as claimed in claim 69, further comprising instructions for selecting a value for n in accordance with a desired throughput rate.

71. A computer readable storage medium as claimed in claim 49, further comprising instructions for storing the raster matrix in a frame buffer.

72. A method of converting a vector video signal into a raster video signal substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings and/or examples.

73. An apparatus for converting a vector video signal into a raster video signal substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings and/or examples.

74. A computer readable storage medium substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings and/or examples.
Figure 1

Raster Based Display

Video Interface

RAM

ROM

Processor/PLA/FPGA

X, Y Deflection Signals

A/D

Figure 1
Figure 2

Deflection signals X, Y

Vector-to-Raster converter [NxM]

Video scaler [N1xM1]

LCD
Figure 3

Diagram showing the process of converting data from ADCs to output on an LCD panel. The diagram includes stages for X and Y ADC codes, digital filters, pixels mapping, frame buffers, summing, and averaging. The output resolution is [NxM] and the final output is [N1xM1].
Figure 4

Averaging

\[
\begin{array}{ccc}
1 & 3 & 1 \\
0 & 1 & 0 \\
0 & 0 & 0 \\
\end{array}
\Rightarrow
\begin{array}{ccc}
0 & 1 & 0 \\
0 & 0 & 0 \\
0 & 0 & 0 \\
\end{array}
\]